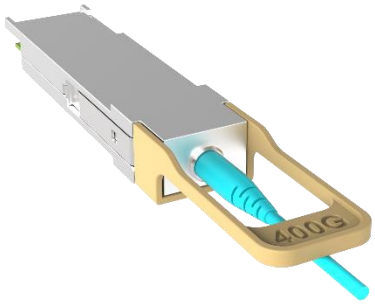
AAQD2QP2400Cxxx

PRODUCT DETAILS:
*Multi-Mode,400GBASE-SR8,QSFP56-DD TO 2*QSFP56*

PRODUCT FEATURES



- Supports 425Gbps
- Single 3.3V Power Supply
- QSFP56-DD End Power dissipation < 10W

  Each QSFP56 End Power Dissipation <5W
- Up to 30m over MMF
- RoHS compliant
- QSFP56-DD/QSFP56 MSA Compliant
- QSFP56-DD:8x26.5625GBd(PAM4) Electrical interface

  QSFP56: 4x26.5625GBd(PAM4) Electrical interface
- VCSEL Transmitter

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- PIN and TIA array on the receiver side
- I2C interface with integrated Digital Diagnostic Monitoring
- Commercial case temperature range of 0°C to 70°

APPLICATIONS

- 400G QSFP56-DD to 2x QSFP56 AOC

Ordering information

Part No.	Data Rate	Fiber	Distance	Temp.	DDMI	CMIS
AAQD2QP2400Cxxx	425Gbps	MMF	1-30m	0~+70℃	Yes	CMIS4.0

Note: xxx means meters.eg. 001 is 1m, max is 30m.s

Product Description

Accelight's QSFP56-DD to 2xQSFP56 AOC is designed for use in 400 Gigabit Ethernet links over 30m MMF. QSFP56-DD end of the AOC module has 8 independent electrical input/output channels operating at 53.125Gbps per channel. Each QSFP56 end of the AOC module has 4 independent electrical input/output channels operating at 53.125Gbps per channel. It consists of two transmitter/receiver units, with each operating on 850nm wavelength. The electrical interface of the module is compliant with the 400GAUI-8/200GAUI-4 interface as defined by IEEE 802.3bs, and compliant with QSFP56-DD/QSFP56 MSA.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	85	°C
Supply Voltage	Vcc	-0.5	3.6	V
Operating Relative Humidity	RH	5	85	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	Tc	0		70	°C
Power Supply Voltage	Vcc	3.135	3.3	3.465	V
Power Supply Noise				25	mVpp
Receiver Differential Data Output Load			100		Ohm
Fiber Length (MMF)				30	m
Bit Error Rate (26.5625GBd PAM4)	BER			2.4E-4	

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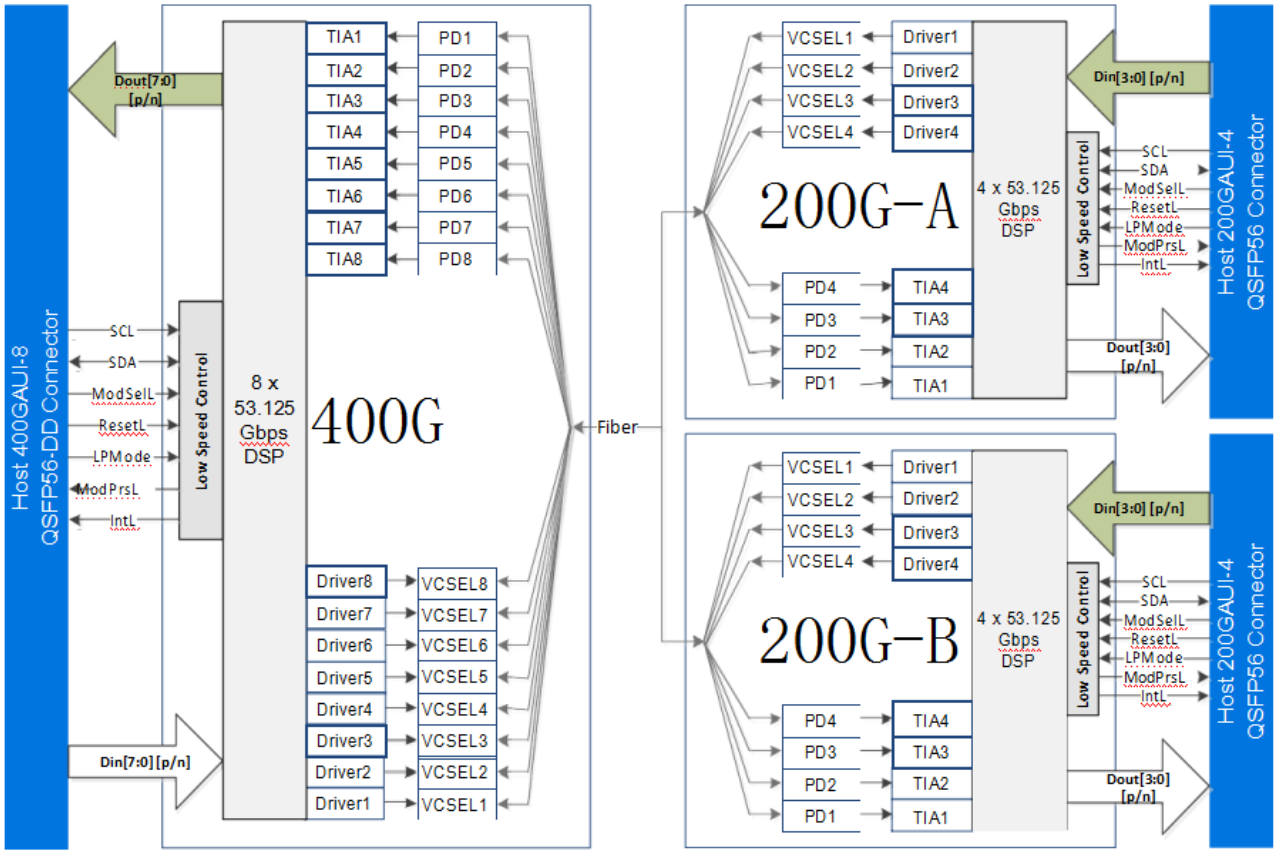

Figure 1: AOC Block Diagram

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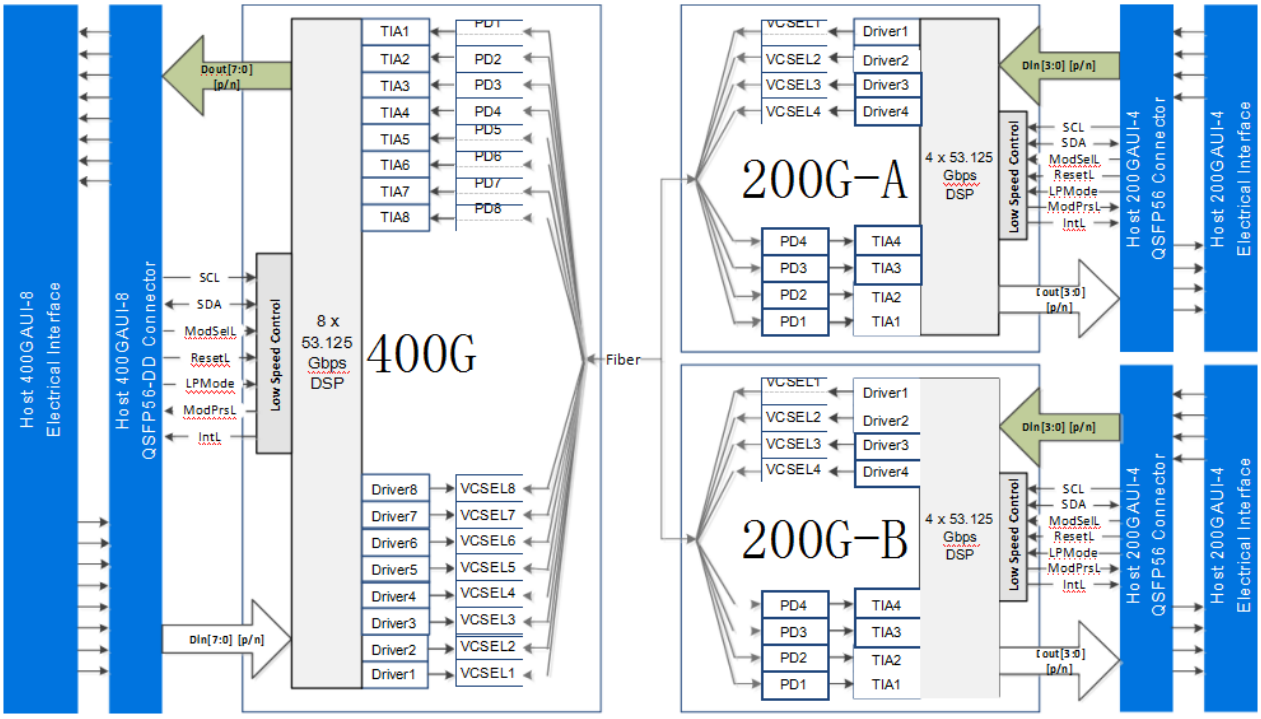


Figure 2: Application Reference Diagram

Transmitter

As shown in Figure 1, the transmitter path of the AOC (QSFP56-DD end) contains an 8x53.125Gbps 400GAUI-8 electrical input with Equalization (EQ) block, two 4-channel laser drivers and multi-mode laser source. And the transmitter path of the AOC (QSFP56 end) contains an 4x53.125Gbps 200GAUI-4 electrical input with Equalization (EQ) block, one 4-channel laser driver and multi-mode laser source.

Receiver

As shown in Figure 1, the receiver path of the AOC (QSFP56-DD end) contains eight PIN photodiodes, two 4-channel trans-impedance amplifiers (TIA) and integrated 400GAUI-8 compliant electrical output blocks. And the receiver path of the AOC (QSFP56 end) contains four PIN photodiodes, one 4-channel trans-impedance amplifier (TIA) and integrated 200GAUI-4 compliant electrical output block.

High Speed Electrical Signal Interface

The interface between QSFP56-DD/QSFP56 module and ASIC/SerDes is shown in Figure 2. The high speed signal lines are internally AC-coupled and the electrical inputs are internally terminated to 100 ohms' differential. All transmitter and receiver electrical channels are compliant to module 400GAUI-8 and 200GAUI-4 specifications per IEEE 802.3bs.

Control Signal Interface

The control signal interface is compliant with QSFP56-DD and QSFP56 MSA. The following pin is provided to control module or display the module status: ModSelL, ResetL, LPMode, ModPrsL and IntL. In addition, there is an industry standard two wire serial interface scaled for 3.3V LVTTL. The definition of control signal interface and the registers of the serial interface memory are defined in the Control Interface & Memory Map section.

Handling and Cleaning

The AOC module may be damaged immediately by exposure to current surges and over voltage events. Care should be taken to restrict exposure to the conditions defined in the Absolute Maximum Ratings. Wave soldering, reflow soldering and/or aqueous wash process with the modules on board are not recommended. Normal handling precautions for electrostatic discharge sensitive devices should be observed.

General Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit
AOC Power Consumption (QSFP56-DD End)				10	W
AOC Power Consumption (QSFP56 End)				5	W
AOC Power Supply Total Current (QSFP56-DD End)				2886	mA
AOC Power Supply Total Current (QSFP56 End)				1515	mA
AC Coupling Internal Capacitor			0.1		µF

Reference Points

Test Point	Description
TP0 to TP5	This channel includes transmitter and receiver differential control impedance printed circuit board insertion loss and cable assembly insertion loss.
TP1 to TP4	All cable assembly measurements are made between TP1 and TP4 as illustrated in Figure 3.

TP0 to TP2 TP3 to TP5	A mated connector pair has been included in both the transmitter and receiver specifications defined in 802.3cd 136.9.3 and 136.9.4. The recommended maximum insertion loss from TP0 to TP2 or from TP3 to TP5 including the test fixture is provided in 802.3cd 136.9.3.2
TP2	Unless specified otherwise, all transmitter measurements defined in 802.3cd 136.9.3 are made at TP2 utilizing the test fixture specified in Annex 136B.
TP3	Unless specified otherwise, all receiver measurements and tests defined in 802.3cd 136.9.4 are made at TP3 utilizing the test fixture specified in Annex 136B.

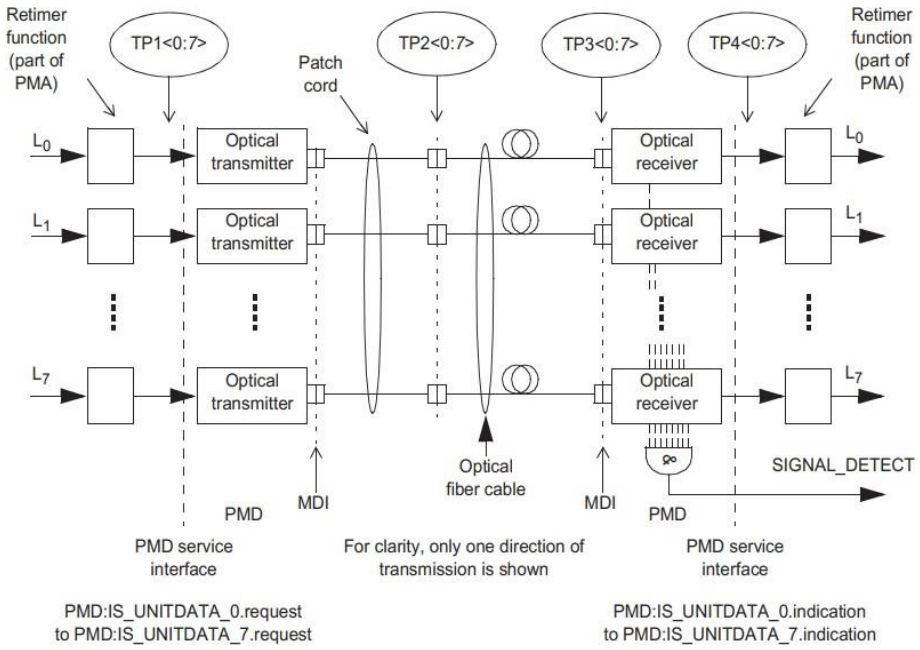


Figure 3: IEEE 802.3cm Block Diagram for 400GBASE-SR8 Transmit/Receive Paths

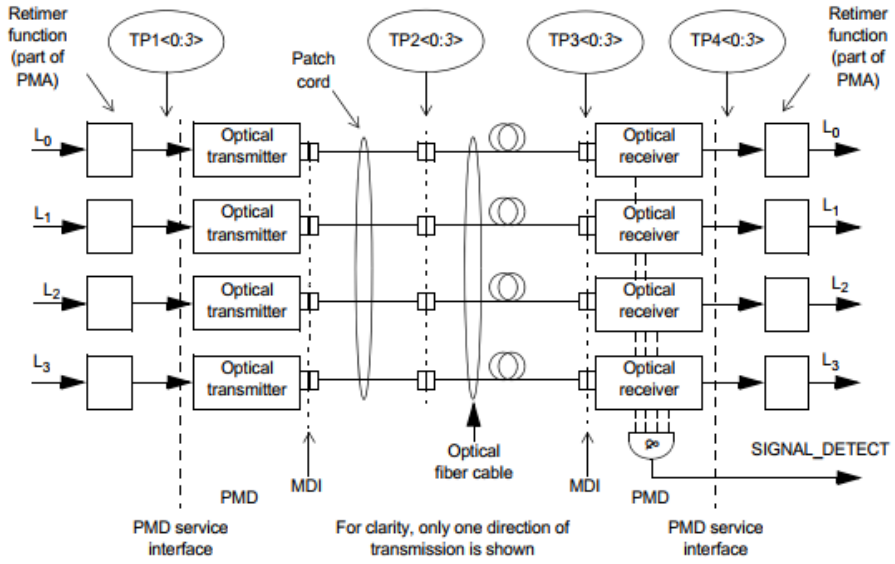


Figure 4: IEEE 802.3cd Block Diagram for 200GBASE-SR4 Transmit/Receive Paths

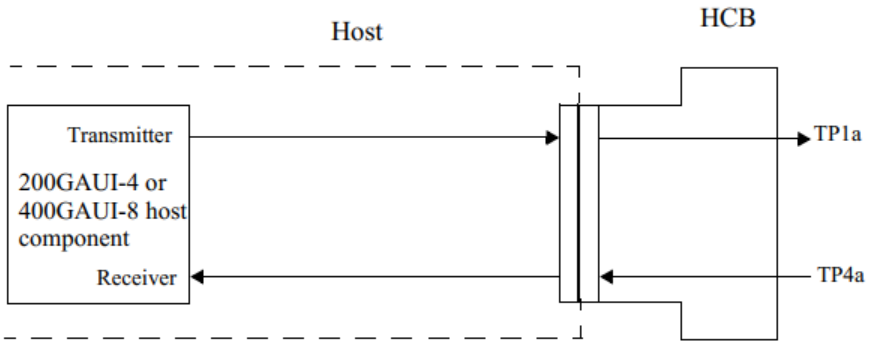


Figure 5: IEEE 802.3bs 400GAUI-8/200GAUI-4 C2M Compliance Points TP1a, TP4a

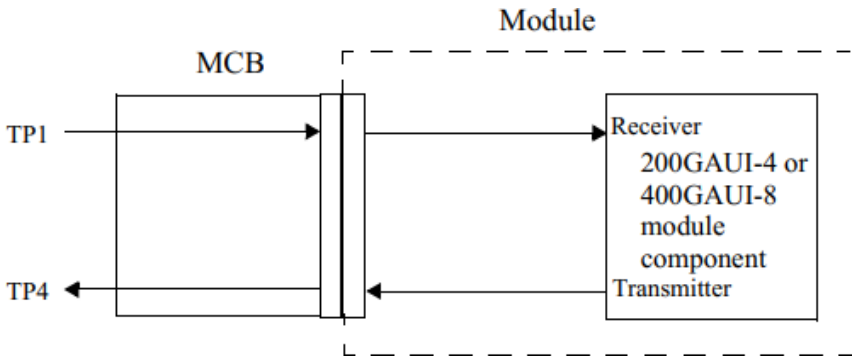


Figure 6: IEEE 802.3bs 400GAUI-8/200GAUI-4 C2M Compliance Points TP1, TP4

High Speed Electrical Input Characteristics

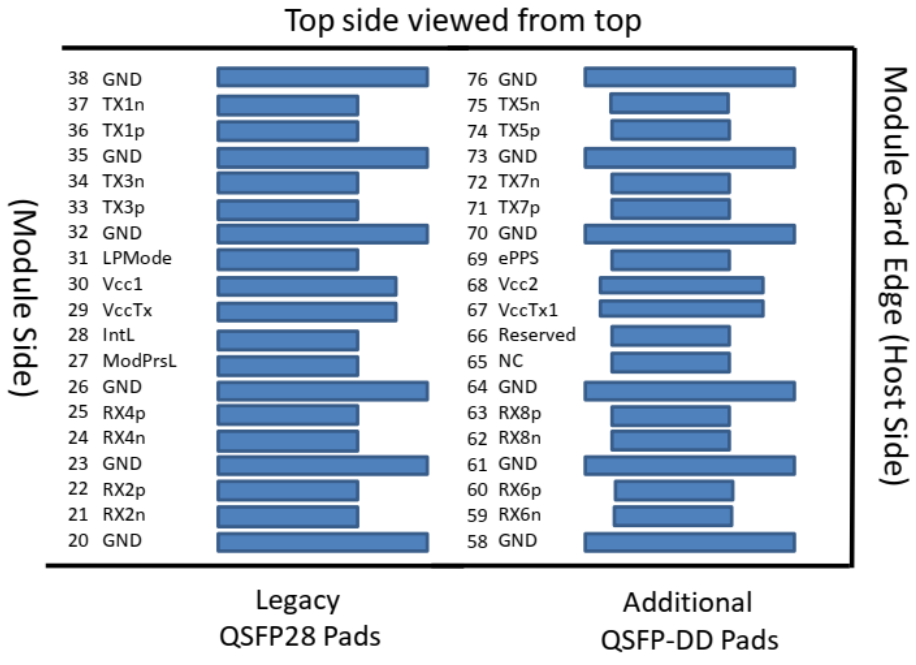
Parameter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate per Lane	TP1		26.5625± 100ppm		GBd
Differential peak-peak Input Voltage Tolerance	TP1a	900			mV
Differential Input Return Loss	TP1	Equation (83E-5)			dB
Common To Differential Mode Conversion Return Loss	TP1	Equation (83E-6)			dB
Differential Termination Mismatch	TP1			10	%
Single-Ended Voltage Tolerance Range	TP1a	-0.4		3.3	V
DC Common-Mode Output Voltage	TP1	-350		2850	mV
Module Stressed Input Test	TP1a				
Eye Width			0.22		UI
Applied peak-peak Sinusoidal Jitter			Table 120E-6		

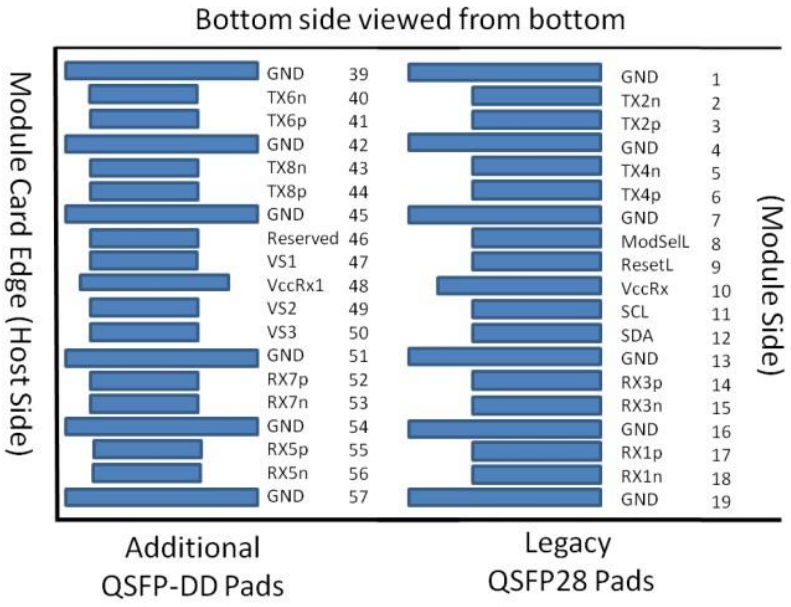
Eye Height			32		mV

High Speed Electrical Output Characteristics

ParamPareter	Test Point	Min.	Typical	Max.	Unit
Signaling Rate per Lane	TP4		26.5625± 100ppm		GBd
AC Common-Mode Output Voltage (RMS)	TP4			17.5	mV
Differential Peak-to-Peak Output Voltage	TP4			900	mV
Near-end ESMW (Eye Symmetry Mask Width)	TP4	0.265			UI
Near-end Eye Height, Differential	TP4	70			mV
Differential Output Return Loss	TP4	Equation (83E-2)			
Common to Differential Mode Conversion Return Loss	TP4	Equation (83E-3)			
sDifferential Termination Mismatch	TP4			10	%
Transition Time (20% ~80%)	TP4	9.5			ps
DC Common Mode Voltage	TP4	-350		2850	mV

QSFP56-DD End Electrical Pad Layout





Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence4	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-	3B	

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			Inverted Data Output		
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	PLMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter	3A	
			Inverted Data Input		
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3

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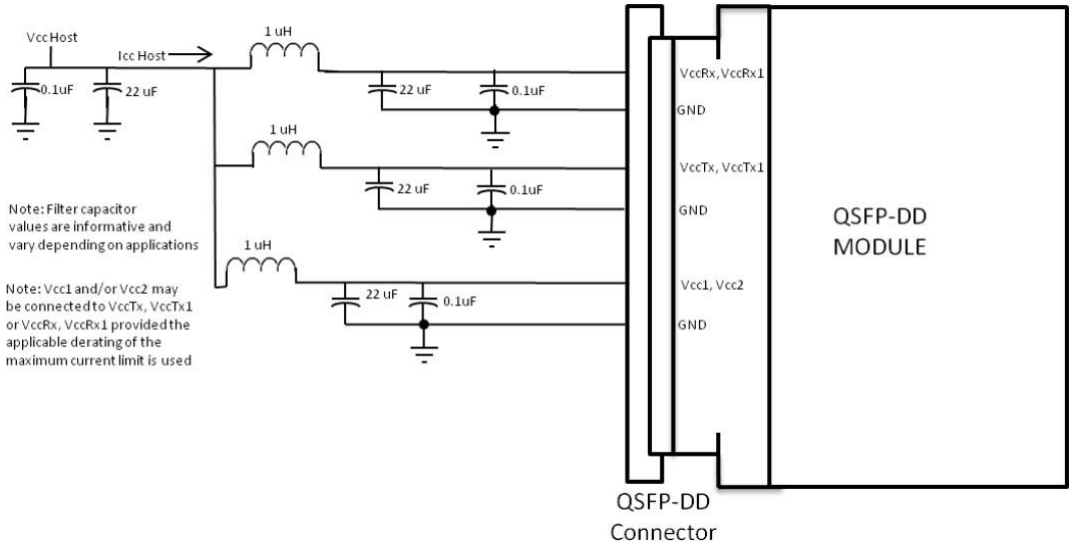
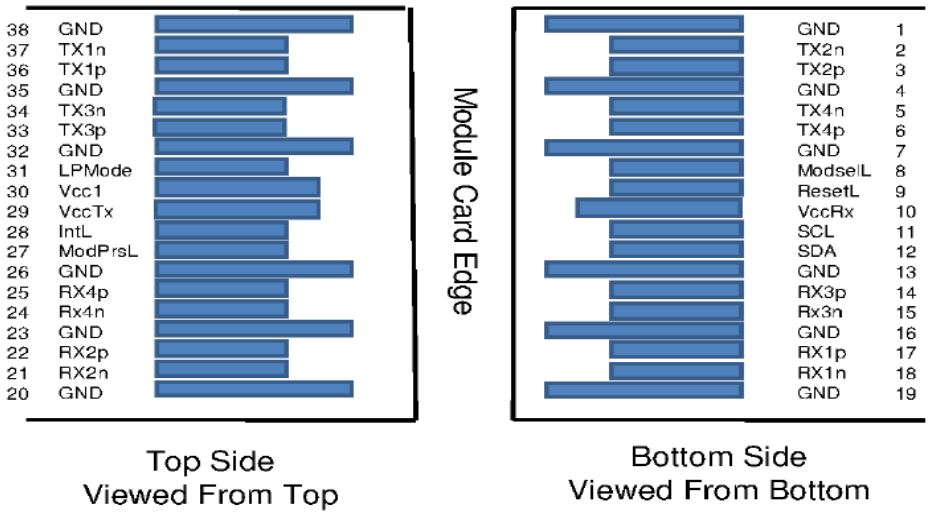
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

1: QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.
3: All Vendor Specific, Reserved and No Connect pins may be terminated with 50 ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 k Ohms and less than 100 pF.
4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.



QSFP56 End Electrical Pad Layout



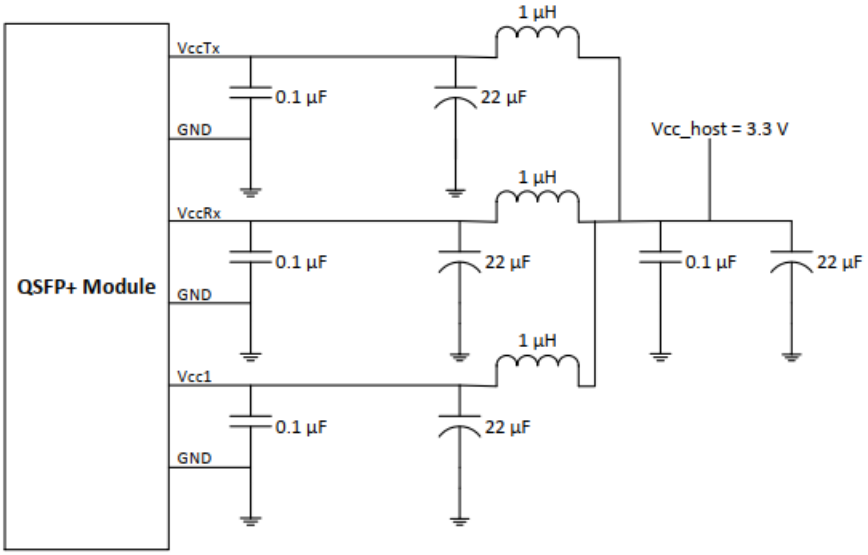
Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS - I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS - I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	

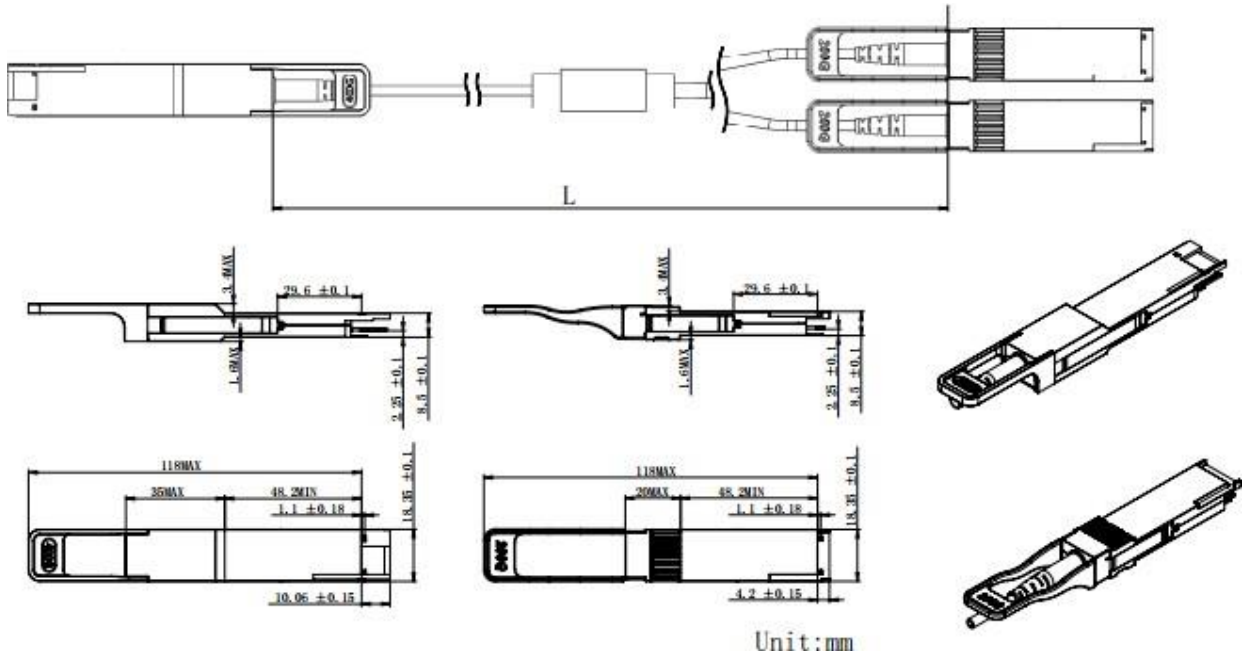
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

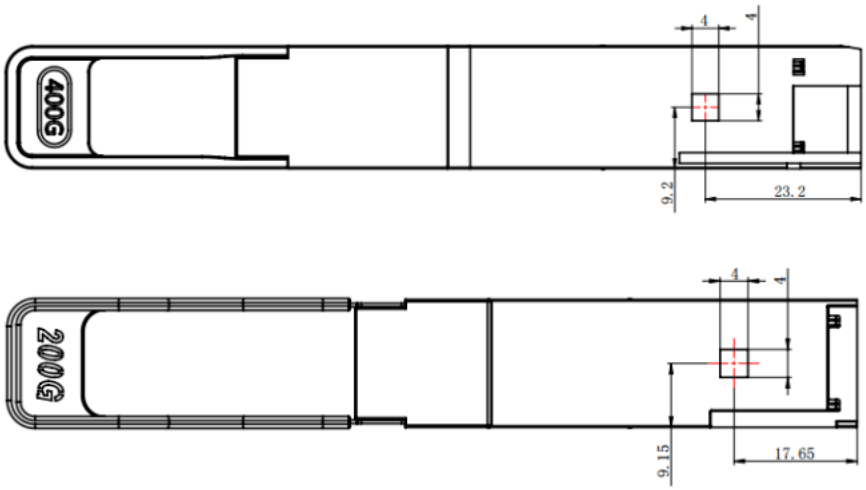
1: GND is the symbol for signal and supply (power) common for the QSFP56 module. All are common within the QSFP56 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in SFF-8679 Table 6. Recommended host board power supply filtering is shown in Figures 12. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP56 Module in any combination.



Mechanical Specifications





Version History

Revision	Description	Release date
1.0	Initial release	Mar 9th ,2022
2.0	Update content according to new template.	Sep 26th,2022

